University	Peter the Great St. Petersburg Polytechnic University
Level of English proficiency	Intermediate (B1)
Educational program and field of the educational program for which the applicant will be accepted	ENGINEERING & TECHNOLOGY 2.3.3. Automation and control in technological processes and production 2.9.4. Transportation process management 2.9.8. Intelligent Transport Systems
List of research projects of the potential supervisor (participation/leadership)	Conducting scientific research and development of general technical requirements for an integrated system in managing and ensuring the safety of train traffic in the Moscow Metro and the Central Transport Hub during the implementation of the Moscow Central Diameters project Investigation of technologies for the synthesis of self-checking computational structures based on redundant codes Methods for the railway automation circuits synthesis with fault-detection based on devices with programmable logic
List of the topics offered for the prospective scientific research	Research of synthesis methods the digital devices with or without memory in particularly concerning self-testing, fault tolerance and safe behavior in failure cases Methodologies development for the integrated control systems synthesis in transport and industry Risk-based approach to organizing transport infrastructure monitoring systems Improving the organizing traffic control methods in railway transport by integrating the permanently installed monitoring systems into process dispatching systems Improving inventory counting method, technical record-keeping, certification, maintenance and operation for motorway and railway transport purposes
	*2.01. Transportation science & technology*
	Supervisor's research interests Methods for the high-reliable and safe control systems synthesis in transport and industry
	Supervisor's specific requirements: Core knowledge in fields of discrete mathematics, electronics, combinatorics, probability theory, mathematical analysis Skills: forecasting and data mining methods; programming language at the n2 (Level 1) according to Programmer Competency Matrix; Software packages for modeling digital

Research supervisor: Dmitry Victorovich Efanov, Doctor of Technical Sciences, Professor of Higher School of Transport, Institute of Mechanical Engineering, Materials and Transport Full member of the International Academy of Transport IEEE Member *(place of thesis defence – Federal State Budget Educational Institution for Higher Education «Emperor Alexander I St. Petersburg State Transport University»)*	systems and transport processes (Multisim, MathLab, AnyLogic, etc.). Supervisor's main publications 1. *Efanov D., Khoroshev V.* Method for Ordering Procedures of Dividing States by Procedures with Two and Three Results Taking into Account Their Cost and Weight of States // SPIIRAS Proceedings. – 2020. – Vol. 19. – Issue 1. – Pp. 218-243. – DOI: 10.15622/sp.2020.19.1.8. 2. *Efanov D.V., Sapozhnikov V.V., Sapozhnikov Vl.V.* Organization of a Fully Self-Checking Structure of a Combinational Device Based on Searching for Groups of Symmetrically Independent Outputs // Automatic Control and Computer Sciences. – 2020. – Vol. 54. – Issue 4. – Pp. 279-290. – DOI: 10.3103/S0146411620040045. 3. *Efanov D.V., Sapozhnikov V.V., Sapozhnikov Vl.V.* Boolean-Complement Based Fault-Tolerant Electronic Device Architectures // Automation and Remote Control. – 2021. – Vol. 82. – Issue 8. – Pp. 1403-1417. – DOI: 10.1134/S0005117921080075. 4. *Sapozhnikov V.V., Sapozhnikov Vl.V., Efanov D.V.* Duplication of Boolean Complements for Synthesis of Fault-Tolerant Digital Devices and Systems // Automatic Control and Computer Sciences. – 2022. – Vol. 56. – Issue 1. – Pp. 1-9. – DOI: 10.3103/S0146411622010096. 5. *Efanov D., Pogodina T.* Properties Investigation of Self-Dual Combinational Devices with Calculation Control Based on
	Results of intellectual activity The self-checking digital devices synthesis theory based on binary sum codes and their modifications has been developed. The bases for the fault-tolerant digital devices synthesis based on code methods for computing control have been developed. Methods have been developed to improve the digital devices controllability through the pulsed operation mode using and calculations control based on the self-duality of the generated functions.